In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Currently Amended) An instruction buffer for a pipeline processor comprising:

a sequence of instructions arranged in an order determined beforehand, wherein respective instructions of said sequence of instructions may include dependencies on other instructions of said sequence of instructions and wherein respective ones of said dependencies may be canceled upon issuance or execution of corresponding ones of said other instructions of said sequence of instructions;

a first buffer including entries arranged in a preselected entry number order for storing respective instructions of said sequence of instructions; and

a second buffer including other entries for storing instructions, wherein an instruction having no uncanceled dependencies, and thus capable of execution, stored in any one of said other entries earlier than other instructions is issued earlier than said other instructions stored in entries of said second buffer,

wherein any one instruction of said sequence of instructions stored in any one of the entries of the first buffer designated by a relatively lower entry number than another instruction in another entry is prior, in order, to another instruction stored in another entry of the first buffer and containing an instruction designated by a relatively higher entry number than said one instruction of said sequence of instructions; and

wherein said first and second buffers are each operable to concurrently issue, in said storage entry

number order in a respective one of said first buffer and said second buffer, instructions having no ~~uncancelled~~ uncanceled dependencies and which are thus capable of execution.

2. (Previously Presented) The instruction buffer as claimed in claim 1, wherein the entries of the first buffer each show whether or not the instruction stored therein is ready to be issued.

3. (Previously Presented) The instruction buffer as claimed in claim 2, wherein the instruction first issued from among the entries of the first buffer whose instructions are ready to be issued is the entry having a lowest storage entry number among said entries of the first buffer whose instructions are ready to be issued.

4. (Previously Presented) The instruction buffer as claimed in claim 3, wherein the entries of the first buffer storing the instructions are lower in entry number than the entries storing no instructions.

5. (Cancelled)

6. (Previously Presented) A method of controlling a buffer queue for a pipeline processor, comprising the steps of:

generating a first group of instructions in a priority order determined beforehand;

generating a second group of instructions belonging to said first group of instructions, respective instructions of said second group of instructions being capable of having dependencies on an instruction of said first group of instructions, said dependencies being

canceled upon issuance of corresponding instructions of said first group of instructions, said instructions of said second group of instructions being capable of being executed if having no uncanceled dependencies; and

executing one instruction of said second group of instructions having no uncanceled dependencies and highest in said priority order among said first group of instructions while executing other instructions which are only in said first group of instructions in said priority order predetermined beforehand.

7. (Previously Presented) The method as claimed in claim 6, further comprising the steps of:

generating a third group of instructions included in said first group of instructions; and

generating a fourth group of instructions included in said first group of instructions and not dependent on said third group of instructions;

wherein when one instruction of said fourth group of instructions highest in priority order does not belong to said second group of instructions, no instruction of said fourth group of instructions is executed.

8. (Previously Presented) The method as claimed in claim 7, wherein one of two instructions belonging to said third group or fourth group of instructions is not executable until the other instruction of said two instructions is executed.

9. (Original) The method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group.

10. (Previously presented) The method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group are operation instructions and memory access instructions, respectively.

11. (Previously Presented) A buffer queue control for a pipeline processor comprising:

a reorder buffer for registering a plurality of instructions in an order of instructions;

a first buffer for storing first instructions included in the plurality of instructions as first entries;

a second buffer for storing, among the plurality of instructions, second instructions other than the first instructions;

a said second instruction including an instruction having a dependency such that said second instruction should be issued after a said first instruction and wherein said dependency is canceled upon issuance of said first instruction corresponding to said dependency;

said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instructions;

said buffer queue control further comprising:

means for releasing any one of the plurality of first entries that stores an instruction that is issued;

means for shifting any one of the first instructions that is not issued to an entry prior, in order, by one;

means for issuing one of the second instructions, which is earliest in said order of instructions and which has no uncanceled dependencies and thus can be executed; and

means for deleting any one of the plurality of

instructions that has been executed and is earlier, in said order of instructions, than instructions not executed.

12. (Previously Presented) The buffer queue control as claimed in claim 11 further comprising means for issuing any one of the first instructions that is earliest in said order of instructions and ready to be issued.

13. (Previously Presented) The buffer queue control as claimed in claim 12, wherein said second buffer comprises a plurality of second entries each for storing a particular one of the second instructions in said order of instructions, and an issuance pointer for controlling issuance of said second instruction, and

wherein said reorder buffer comprises a head pointer indicative of an entry that has been issued last.

14. (Previously presented). The buffer queue control as claimed in claim 13, wherein one of first instructions can be executed at the same time as one of second instructions.

15. (Previously presented) The buffer queue control as claimed in claim 14, wherein the first instructions comprise operation instructions while the second instructions comprise memory access instructions.

16. (Previously Presented) The instruction buffer as claimed in claim 1, wherein said sequence of instructions are stored in accordance with respective dependencies, wherein said reorder buffer detects dependence of any one instruction of said sequence of instructions on another one instruction of said sequence of instructions, and wherein said dependency is reset upon satisfaction of said dependency by issuance of said another one instruction.